SWITCH WITH LINECARDS QUEUES, AND THRESHOLDS
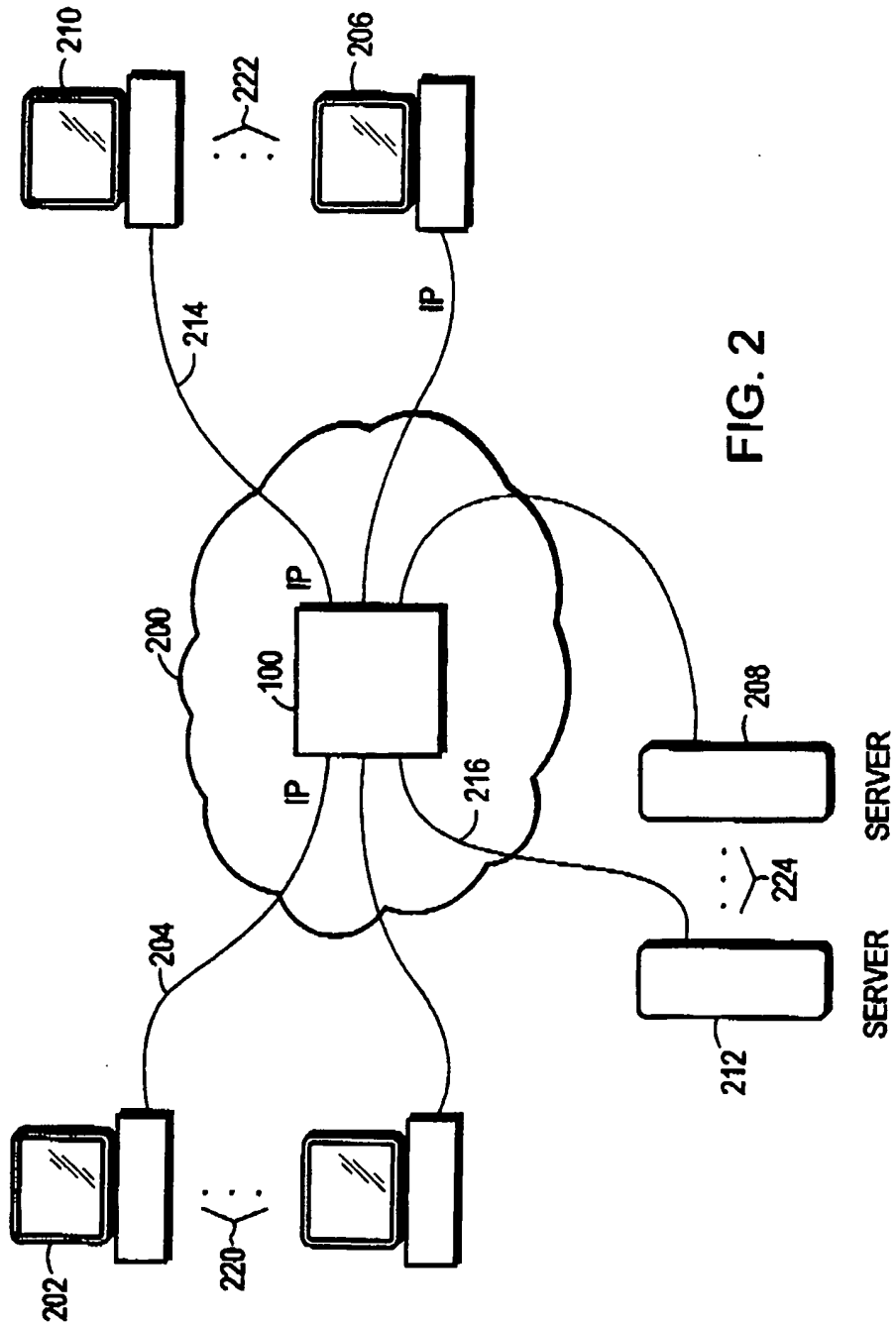
FIG. 1
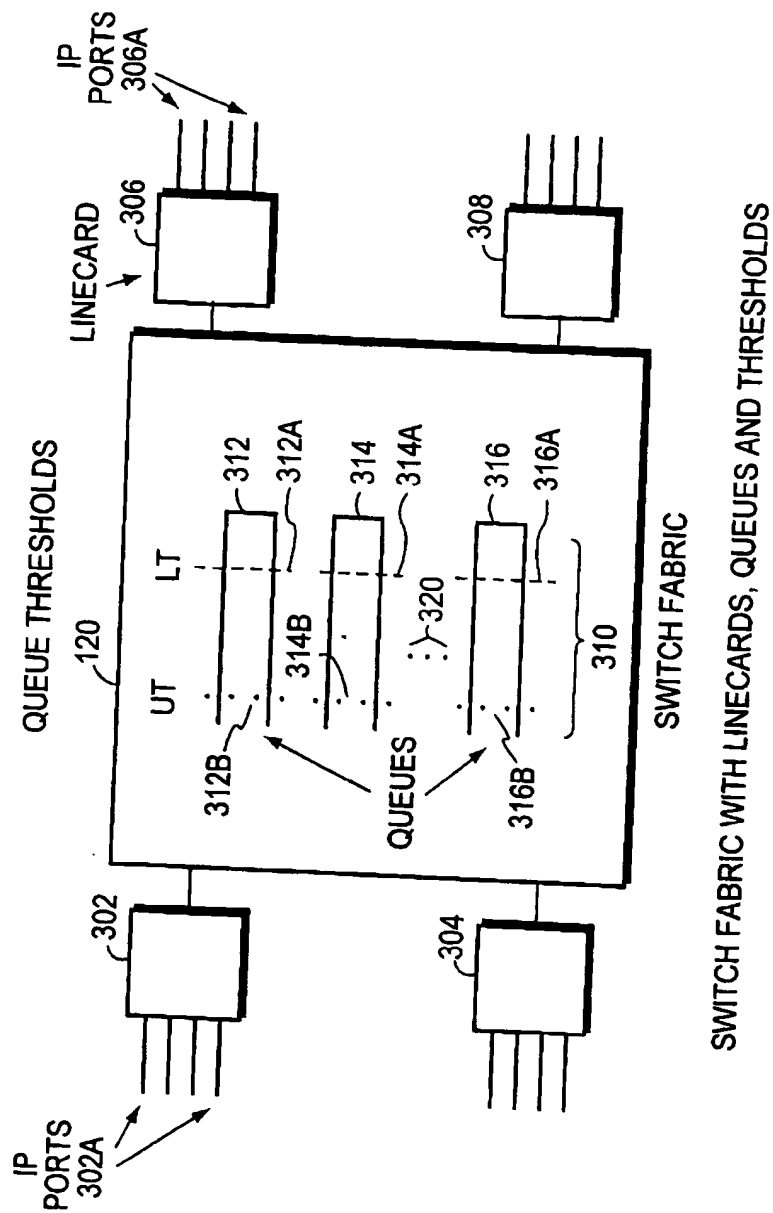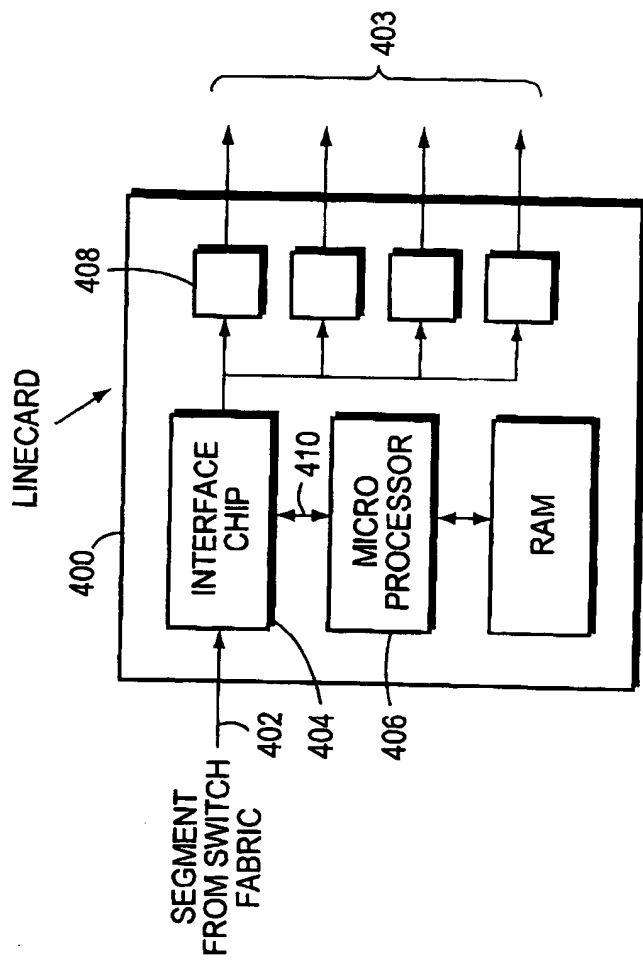
FIG. 2

FIG. 3

SWITCH FABRIC WITH LINECARDS, QUEUES AND THRESHOLDS

LINECARD WITH MICRO-PROCESSOR FOR EXECUTING RED ALGORITHM,
RAM MEMORY FOR STORING CODE AND DATA

FIG. 4

500
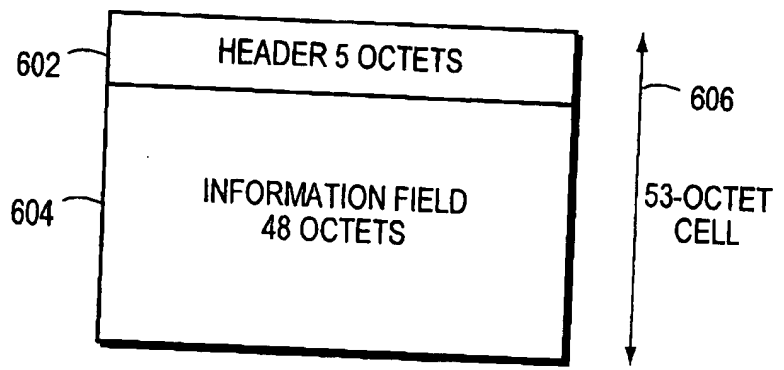
IP PACKET

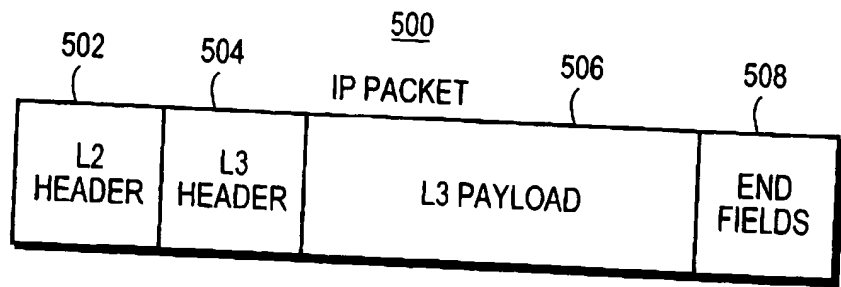| 502	504		506	508
L2 HEADER	L3 HEADER	L3 PAYLOAD		END FIELDS

FIG. 5

600

602	HEADER 5 OCTETS
604	INFORMATION FIELD 48 OCTETS

606

53-OCTET CELL

ATM CELL STRUCTURE

FIG. 6

605

	8	7	6	5	4	3	2	1
606	GENERIC FLOW CONTROL				VIRTUAL PATH IDENTIFIER			
608	VIRTUAL PATH IDENTIFIER				VIRTUAL CHANNEL IDENTIFIER			
610	VIRTUAL CHANNEL IDENTIFIER							
612	VIRTUAL CHANNEL IDENTIFIER				PTI 0	PTI 1	PTI 2	CELL LOSS PRIORITY
614	HEADER ERROR CONTROL							

620   622   624   626

602

ATM CELL HEADER

FIG. 7

FIG. 8

900
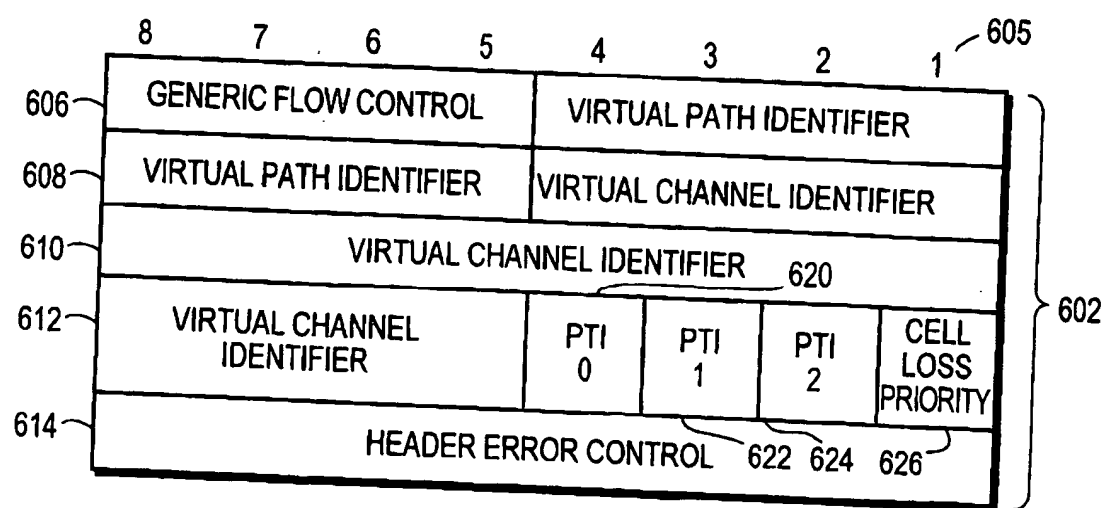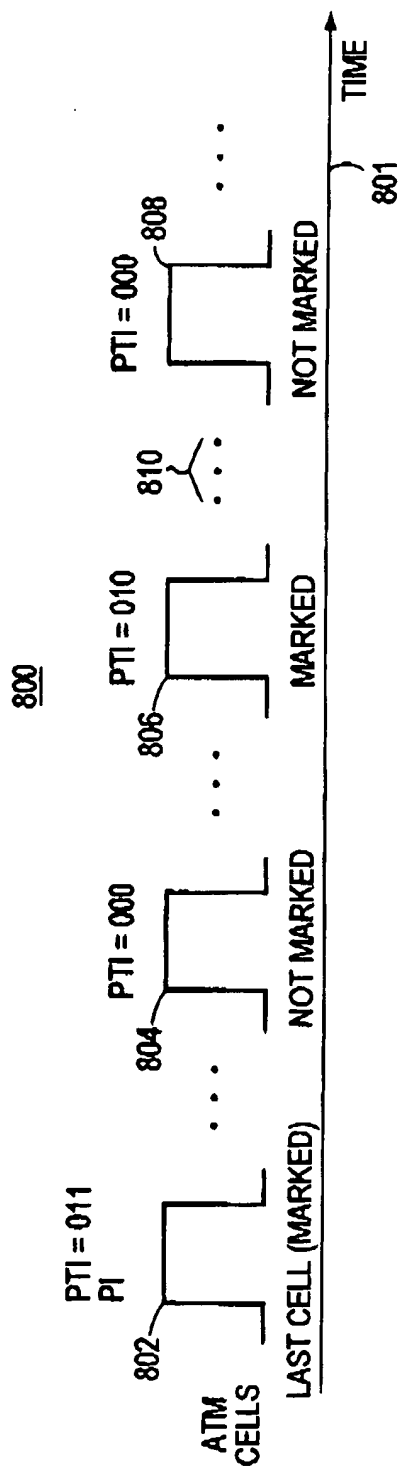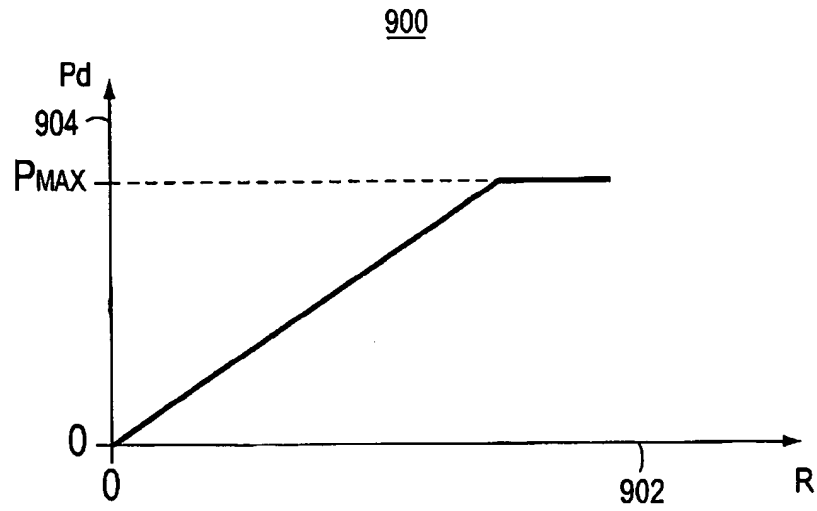
FIG. 9
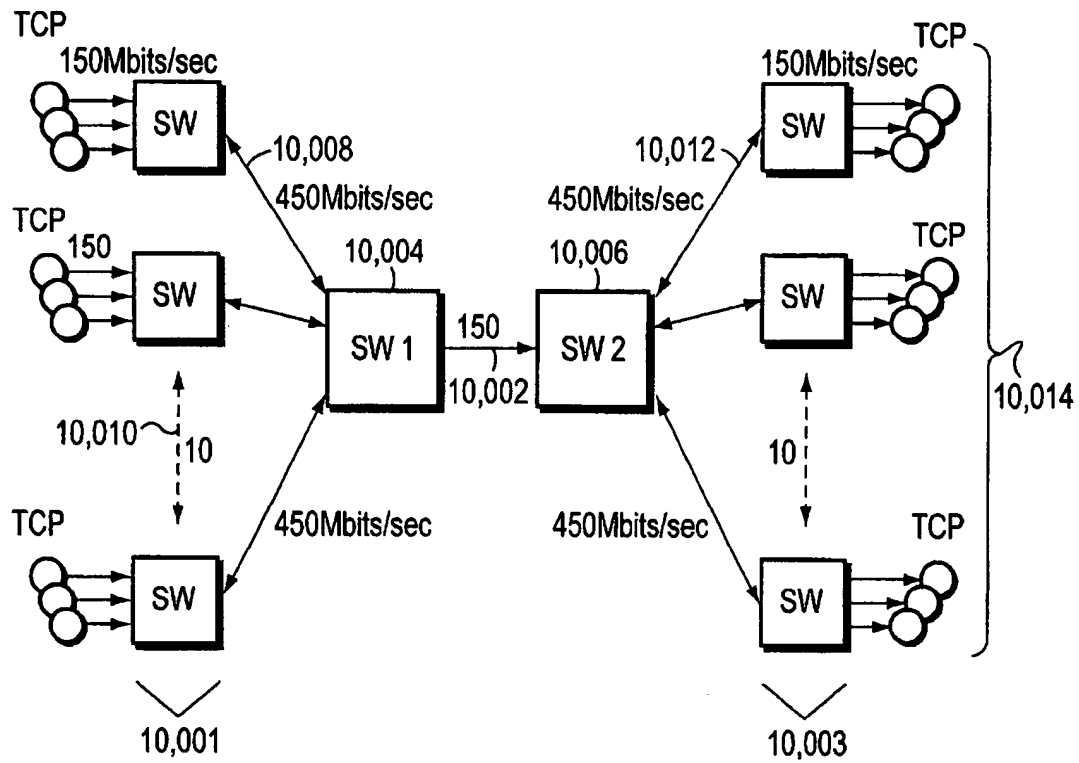
TOPOLOGY FOR RED SIMULATIONS

FIG. 10
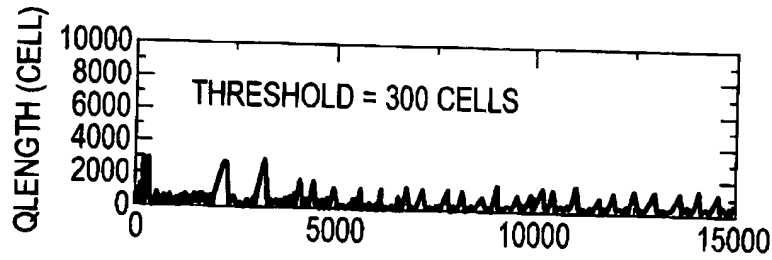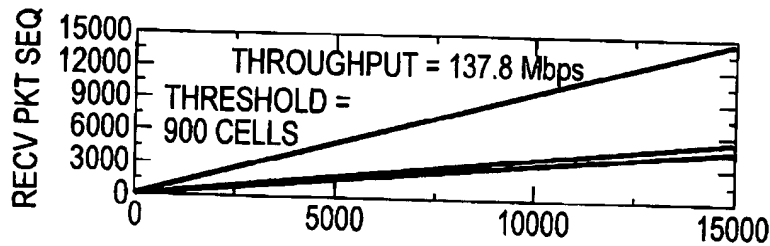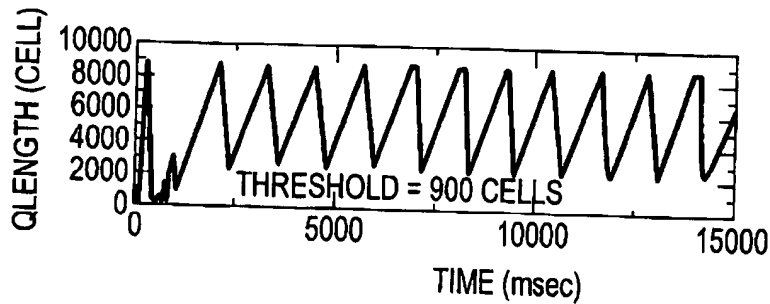
RESULTS FOR EPD-THRESHOLD = 300, 900
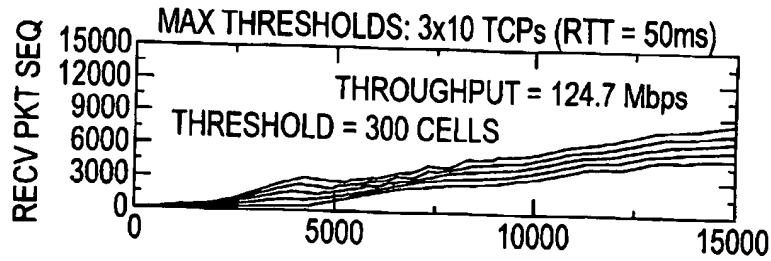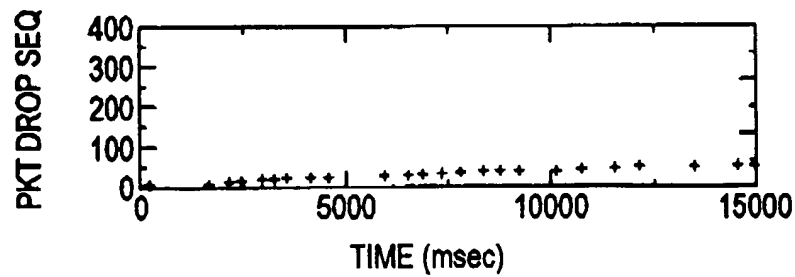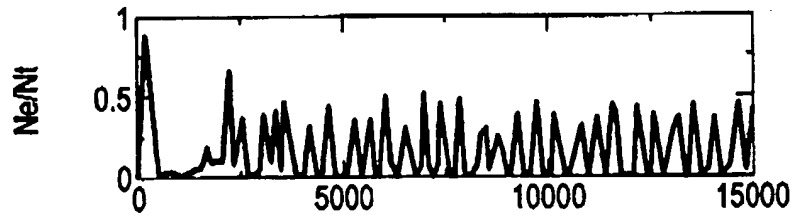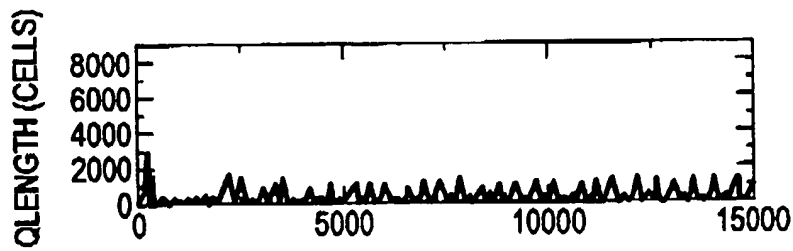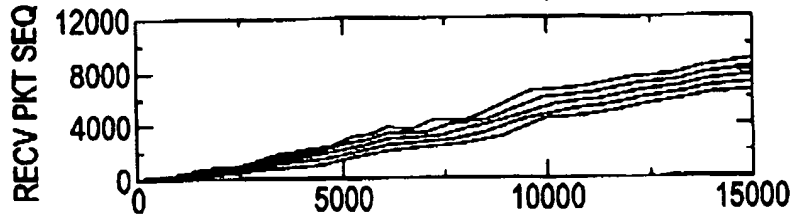
RED: 3x10 TCPs (RTT = 50ms)
Qth=100/300; MAXP=0.01; FREEZE=100ms;
THRUPUT=128.7 Mbps

FIG. 12A

FIG. 12B

FIG. 12C

FIG. 12D

TIME (msec)

RESULTS FOR EFCI-THRESHOLD = 100,
EPD = 300

RED: 3x10 TCP (RTT = 50ms)
Qth=300/900; MAXP=0.01; FREEZE=100ms;
THRUPUT=137.2 Mbps

FIG. 13A

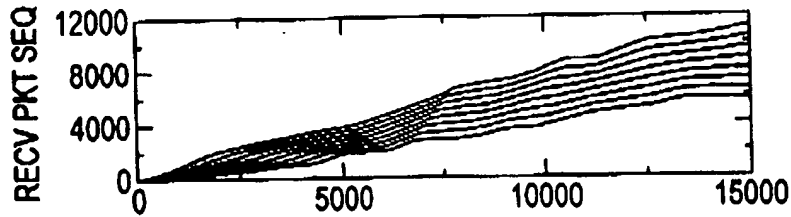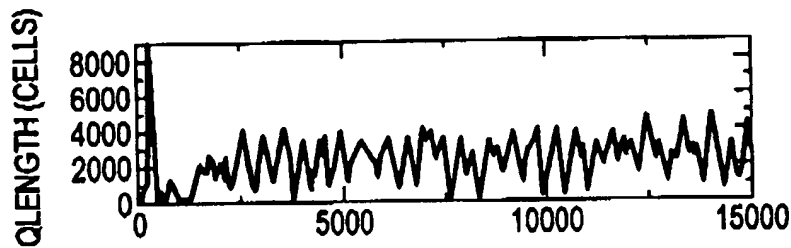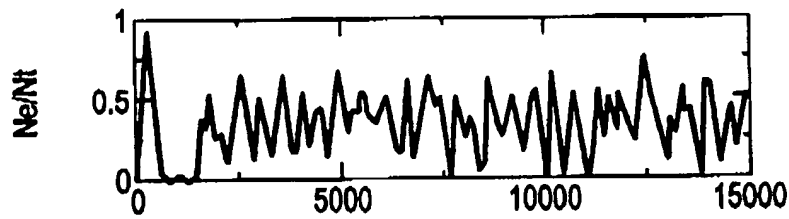**FIG. 13B**
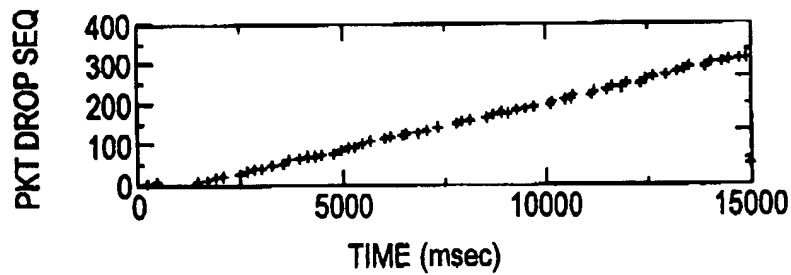
FIG. 13C

FIG. 13D

TIME (msec)
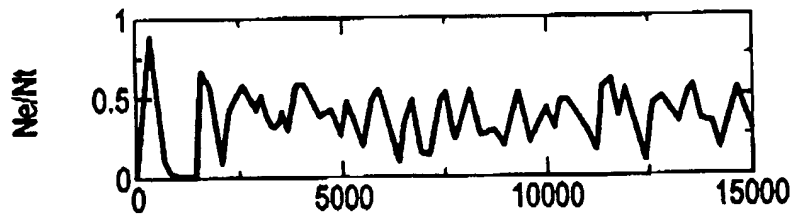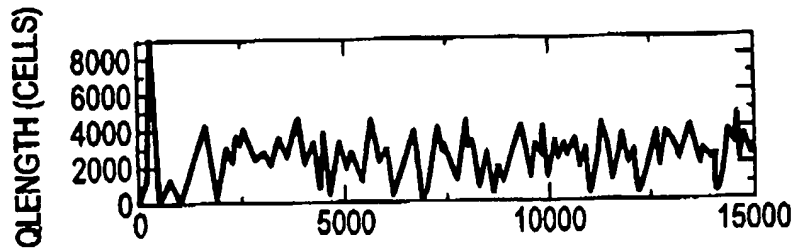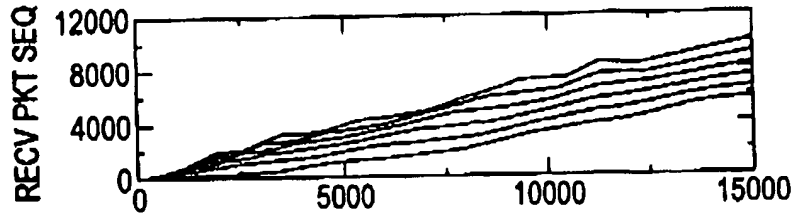
RESULTS FOR EFCI-THRESHOLD = 300,
EPD = 900

RED: 3x10 TCP (RTT = 50ms)
Qth=300/900; MAXP=0.01; FREEZE=200ms;
THRUPUT=137.3 Mbps

FIG. 14A

FIG. 14B

FIG. 14C

FIG. 14D

TIME (msec)
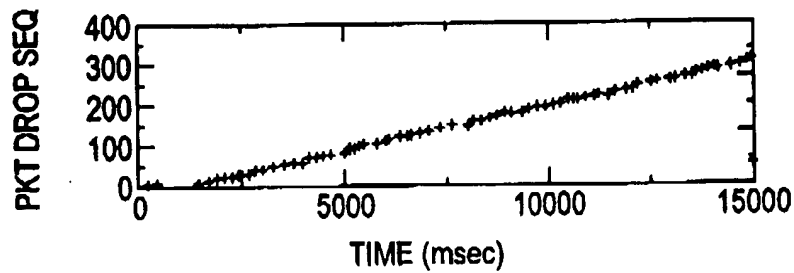
RESULTS FOR PD UPDATE INTERVAL = 200 msec

RED: 10/20 (Hi/Lo) TCPs (RTT = 50ms)
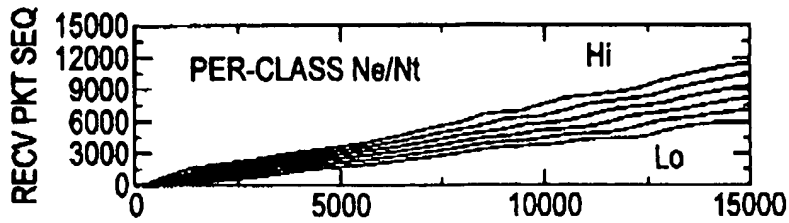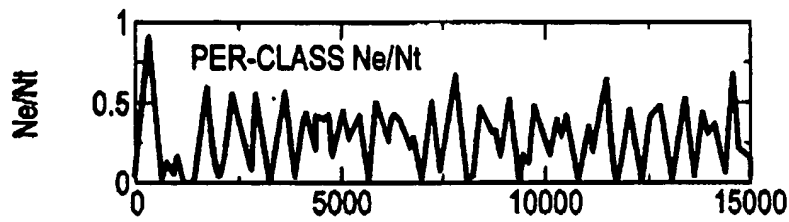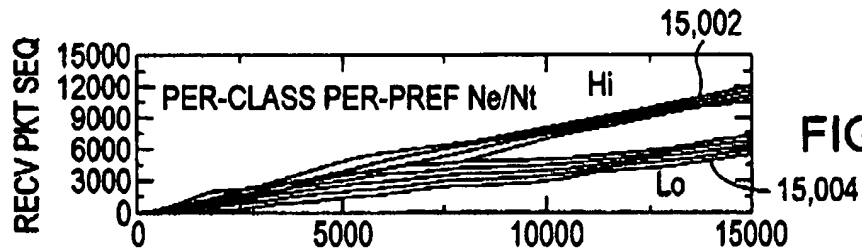PER-CLASS VS. PER-CLASS PER-PREF RATIOS; MAXP=1.0/2.0%
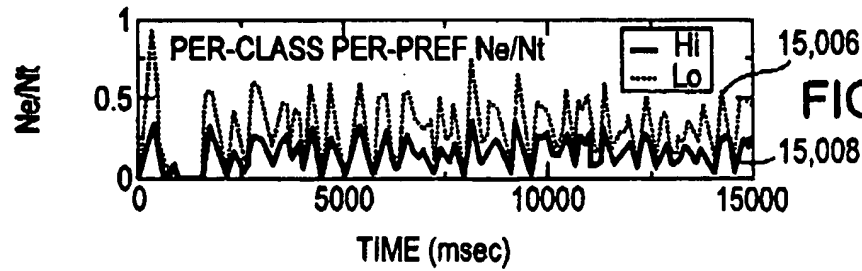

FIG. 15A

FIG. 15B

FIG. 15C

FIG. 15D

TIME (msec)

PER-CLASS VS. PER-CLASS PER-PREFERENCE Ne/Nt